A Novel Time-to-Digital Converter Architecture Based on Coding Theory

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Outline

- Research Objective & Background
- Flash TDC and Problems
- Coding Theory
- Coding Theory based TDC
- FPGA Implementation
- Conclusion

Research Objective

Objective

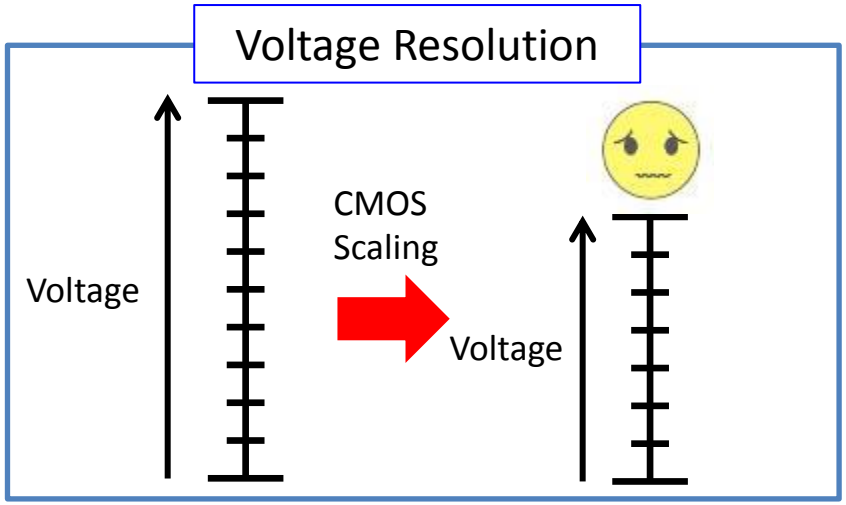
- Development of
  Time-to-Digital Converter (TDC) architecture
  with high-speed and small hardware

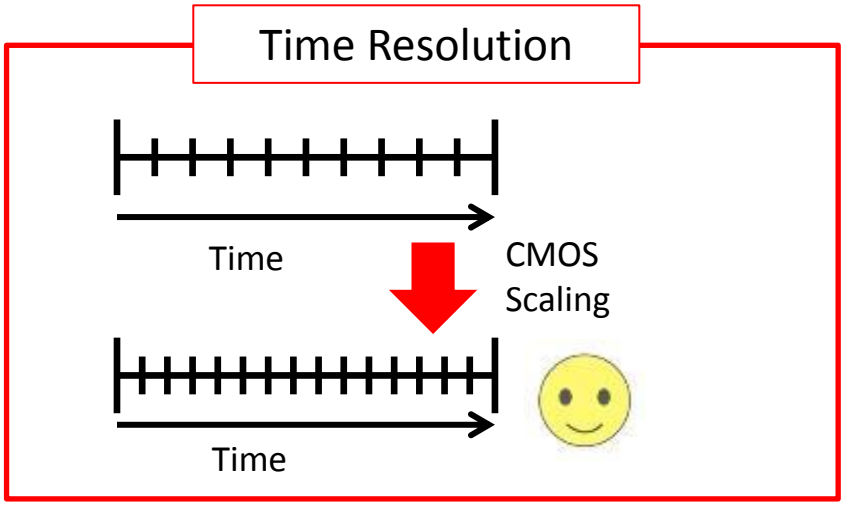
Approach

- Utilization of coding theory

Research Background

TDC plays an important role in nano-CMOS era



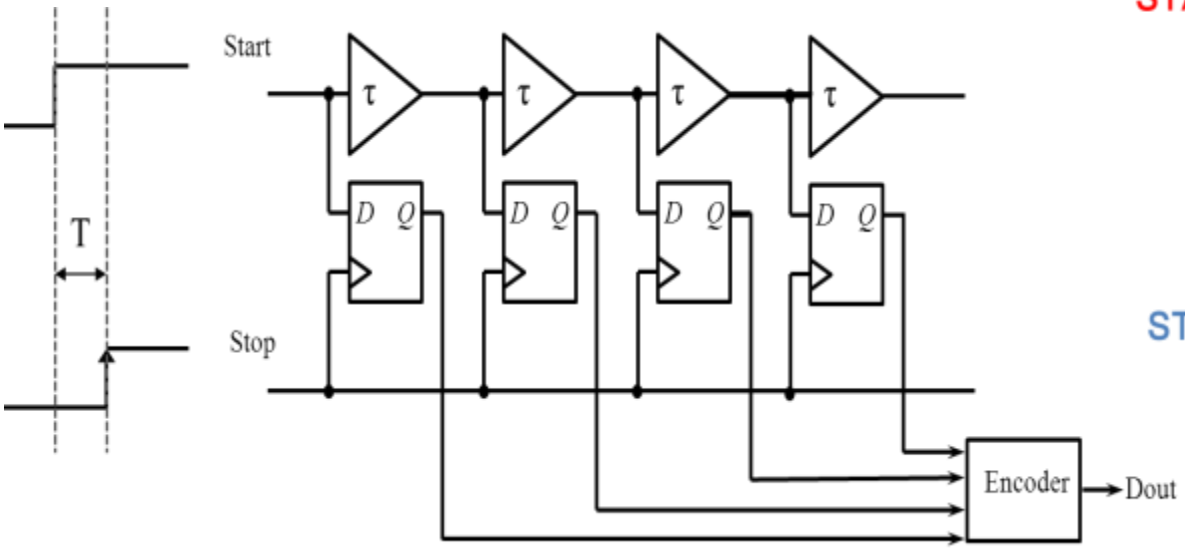


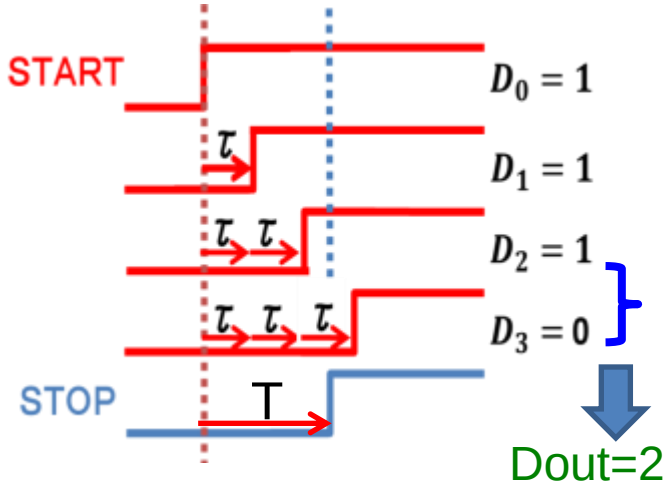
Voltage-domain resolution facing difficulties due to reduced supply voltage

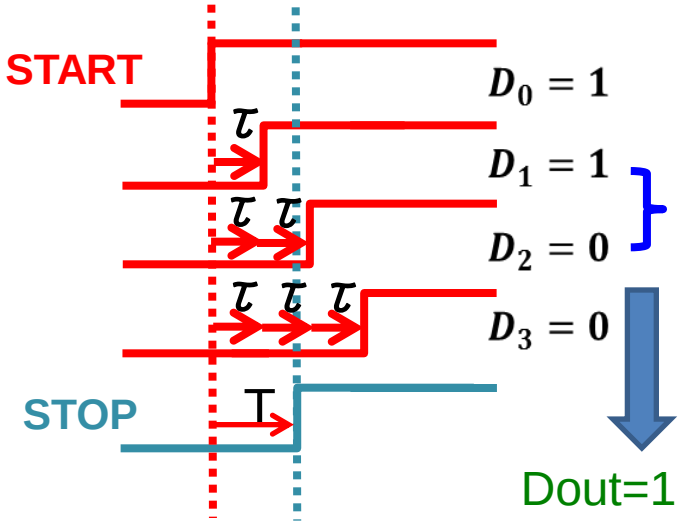
Time-domain resolution becoming superior

TDC measures time interval between two signal transitions, into digital signal.
(widely used in ADPLLs, jitter measurements, time-domain ADC)

Flash TDC







- Digital output (Dout) proportional to time difference between rising edges (T)
- Time resolution τ

Problems of Flash TDC

An n-bit flash TDC with 2^n quantization levels

Advantages

- High-speed timing measurement
- Single-event timing measurement
- All digital implementation

Disadvantages

- 2^n-1 delay elements, 2^n-1 Flip-Flops
- n-bit thermometer-to-binary code encoder

Large circuits
High power consumption

Coding Theory (1/3)

Gray Code

a binary numeral system where two successive values differ in only one bit

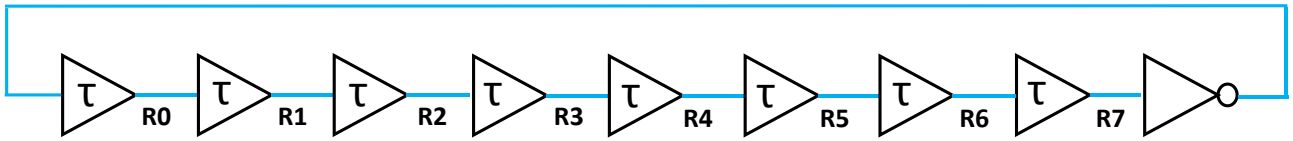
Table. 4-bit Gray Code

Decimal numbers	Binary Code	Gray Code
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0010
4	0100	0110
5	0101	0111
6	0110	0101
7	0111	0100
8	1000	1100
9	1001	1101
10	1010	1111
11	1011	1110
12	1100	1010
13	1101	1011
14	1110	1001
15	1111	1000

- For Gray code, between any two adjacent numbers, only one bit changes at a time
- Gray code data is more reliable compared with binary code

Coding Theory (2/3)

In a ring oscillator, between any two adjacent states, only one output changes at a time. This characteristic is very similar to Gray code.



8-stage Ring Oscillator Output								4-bit Gray Code			
R0	R1	R2	R3	R4	R5	R6	R7	G3	G2	G1	G0
0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	0	0	0	0	1
1	1	0	0	0	0	0	0	0	0	1	1
1	1	1	0	0	0	0	0	0	0	1	0
1	1	1	1	0	0	0	0	0	1	1	0
1	1	1	1	1	0	0	0	0	1	1	1
1	1	1	1	1	1	0	0	0	1	0	1
1	1	1	1	1	1	1	0	0	1	0	0
1	1	1	1	1	1	1	1	1	1	0	0
0	1	1	1	1	1	1	1	1	1	0	1
0	0	1	1	1	1	1	1	1	1	1	1
0	0	0	1	1	1	1	1	1	1	1	0
0	0	0	0	1	1	1	1	1	0	1	0
0	0	0	0	0	1	1	1	1	0	1	1
0	0	0	0	0	0	1	1	1	0	0	1
0	0	0	0	0	0	0	1	1	0	0	0

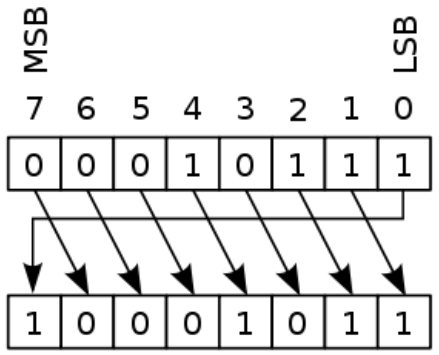
For any given Gray code, its each bit can be generated by a certain ring oscillator.

Coding Theory (3/3)

Cyclic code

a cyclic code is a block code, where the circular shifts of each code-word gives another word that belongs to the code.

Figure. Cyclic code



- Cyclic code can be applied to generate the lower bits of Gray code, which can reduce the frequency of the outputs

Table. Cyclic code with code-word 00001111

State	Cyclic code with code-word 00001111							
	C0	C1	C2	C3	C4	C5	C6	C7
0	0	0	0	0	1	1	1	1
1	1	0	0	0	0	1	1	1
2	1	1	0	0	0	0	1	1
3	1	1	1	0	0	0	0	1
4	1	1	1	1	0	0	0	0
5	0	1	1	1	1	0	0	0
6	0	0	1	1	1	1	0	0
7	0	0	0	1	1	1	1	0

Cyclic Code		Gray Code
C1	is the same as	G1
C0 XOR C1	is the same as	G0

Coding Theory based TDC Architecture (1/2)

A coding theory TDC architecture can be conceived based on Gray code:

- the upper Gray code bits are generated by grouping a few ring oscillators
- the lower Gray code bits are conceived by cyclic code generators, in order to reduce the frequency of the output

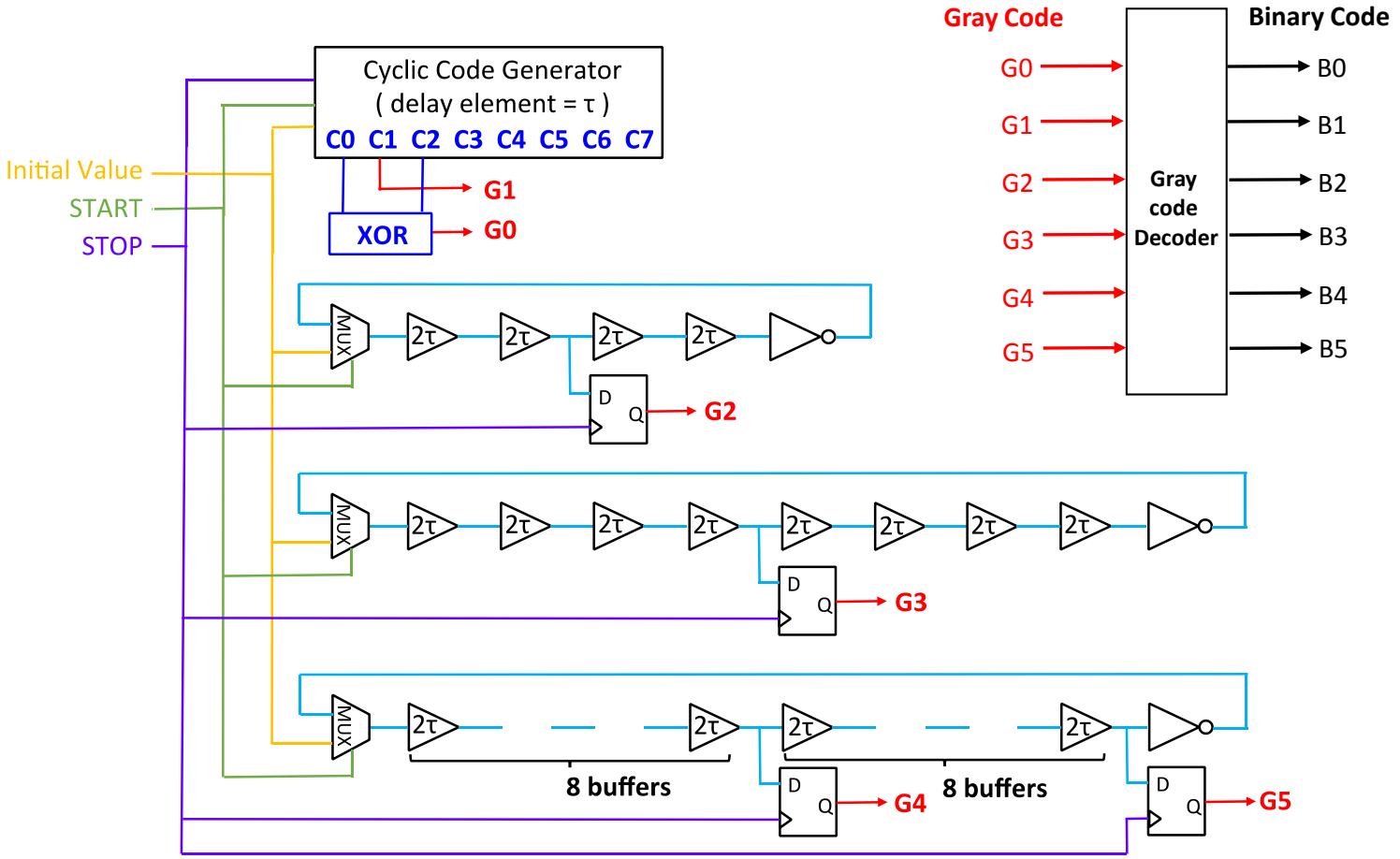


Figure. Proposed 6-bit coding theory based TDC

Coding Theory based TDC Architecture (2/2)

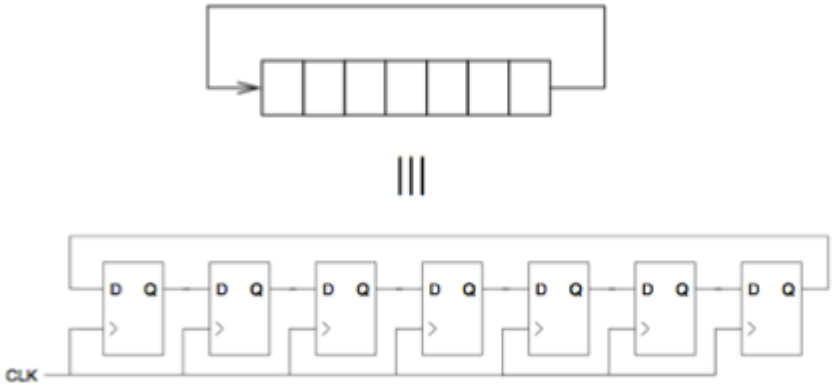


Figure. Generator structure for 8-bit cyclic code

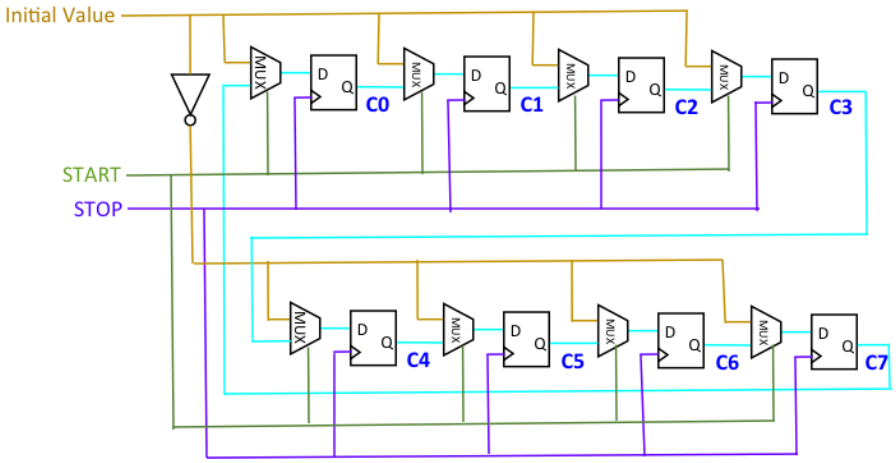
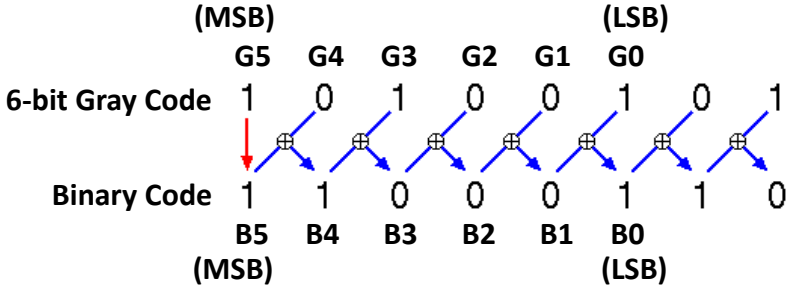


Figure. Circuit diagram of 8-bit cyclic code generator



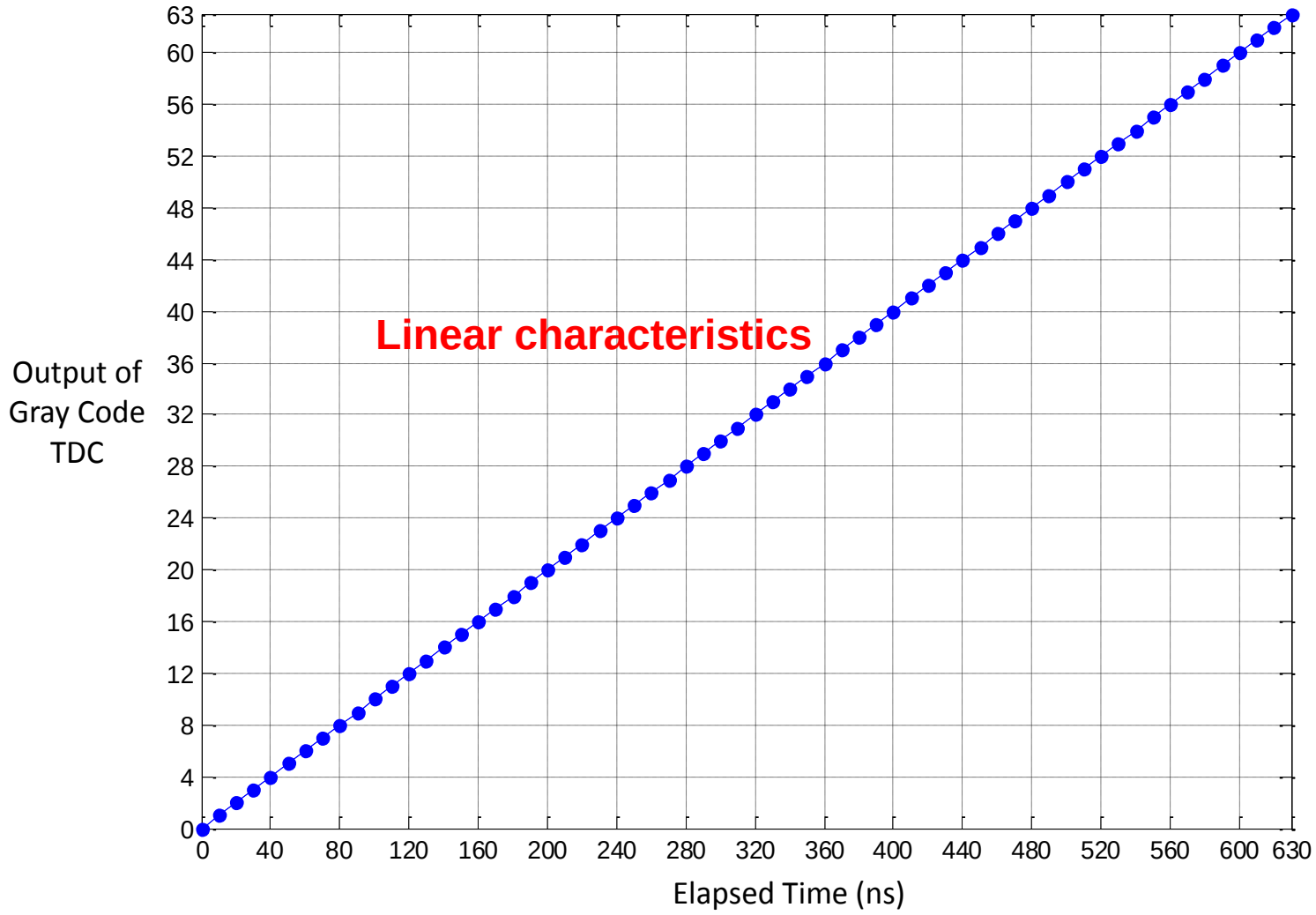
B5=G5
B4=B5 ⊕ G4
B3=B4 ⊕ G3
B2=B3 ⊕ G2
B1=B2 ⊕ G1
B0=B1 ⊕ G0

Figure. Gray code decoder

FPGA Implementation (1/2)

Proposed TDC implementation on Xilinx FPGA

FPGA Implementation (2/2)



Measurement results of the proposed TDC with FPGA.

Proposed TDC operation is confirmed with FPGA evaluation.

Conclusion

We have proposed a code theory based TDC architecture

- Comparable performance to Flash TDC
- Significant hardware & power reduction

- the proposed code theory TDC uses only 28 delay cells and 14 flip-flops, and the maximum stage of the ring oscillator is 16
- while the corresponding flash TDC requires 64 delay cells and 64 flip-flops, and the maximum stage of the ring oscillator is 64

We have implemented the proposed TDC with FPGA

➡ Confirmed its operation